









# Semiconductor device and method for manufacturing the same

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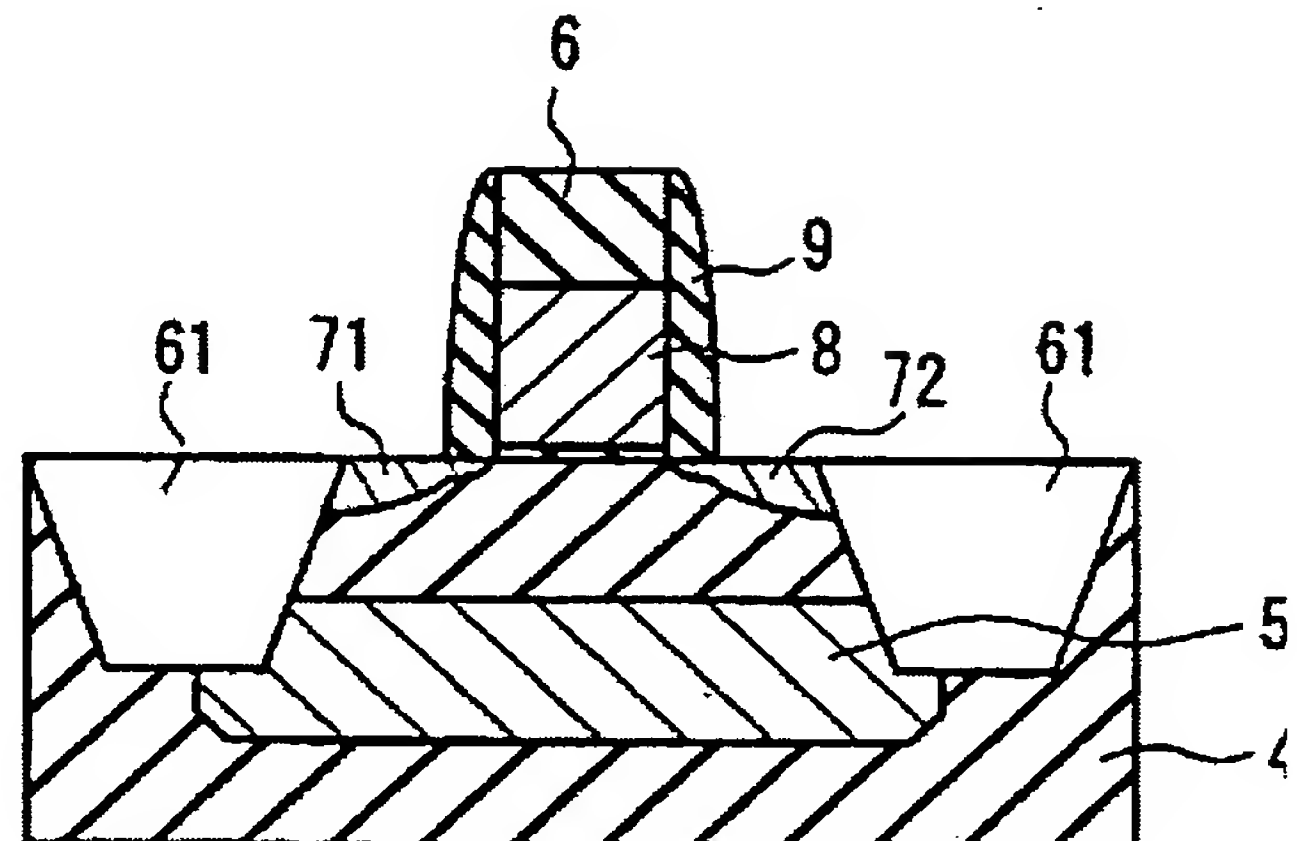
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## Abstract of EP1347503

A semiconductor device includes a gate insulating film (1) formed on a silicon substrate (41), a gate electrode (8) formed on the gate insulating film (1), and an electrical insulating film (6) formed on the gate electrode (8). The electrical insulating film (6) includes a N-H bond and substantially no Si-H bond. The electrical insulating film (6) is formed by using tetrachlorosilane (SiCl<sub>4</sub>) that contains no hydrogen (H) as a source gas for a silicon nitride film. Thus, the semiconductor device can suppress residual hydrogen in the gate insulating film and prevent interface defects of the gate insulating film, a shift in the threshold voltage of a transistor, and the degradation of an on-state current. A method for manufacturing the semiconductor device also is provided.



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EP 1 347 503 A2

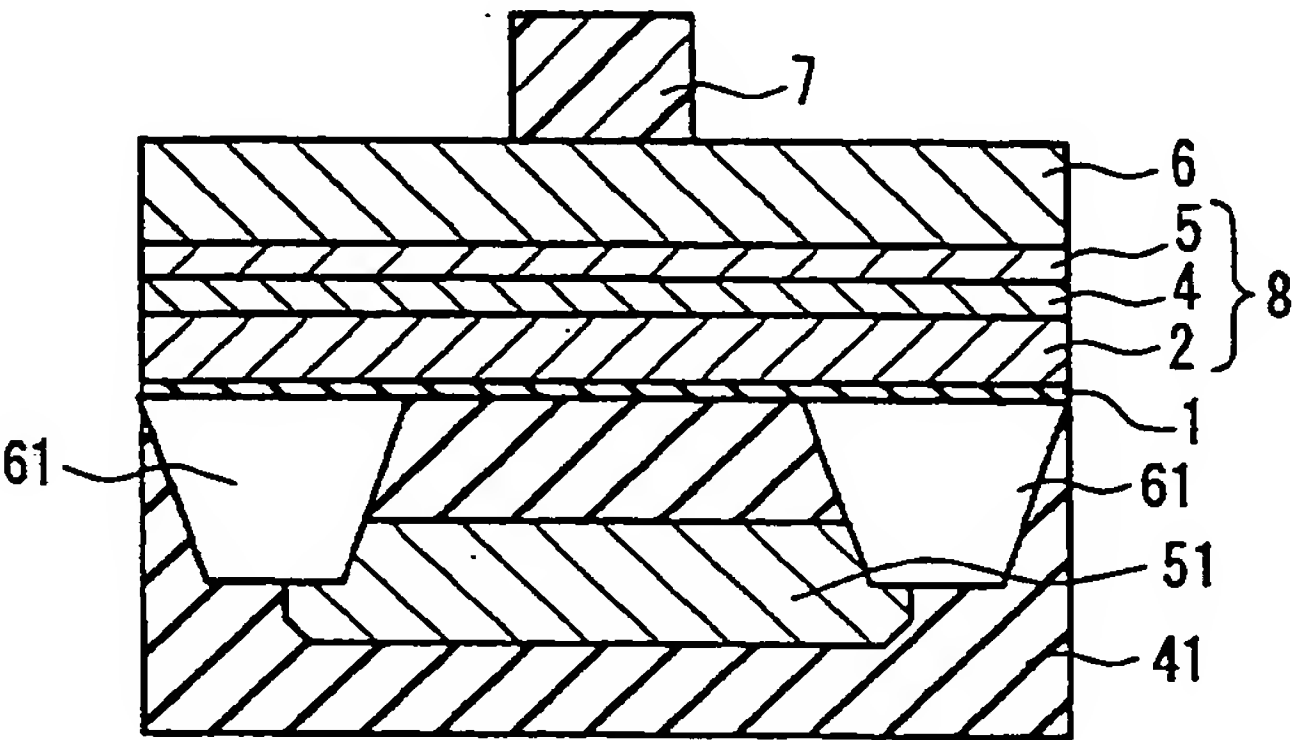


FIG. 1B

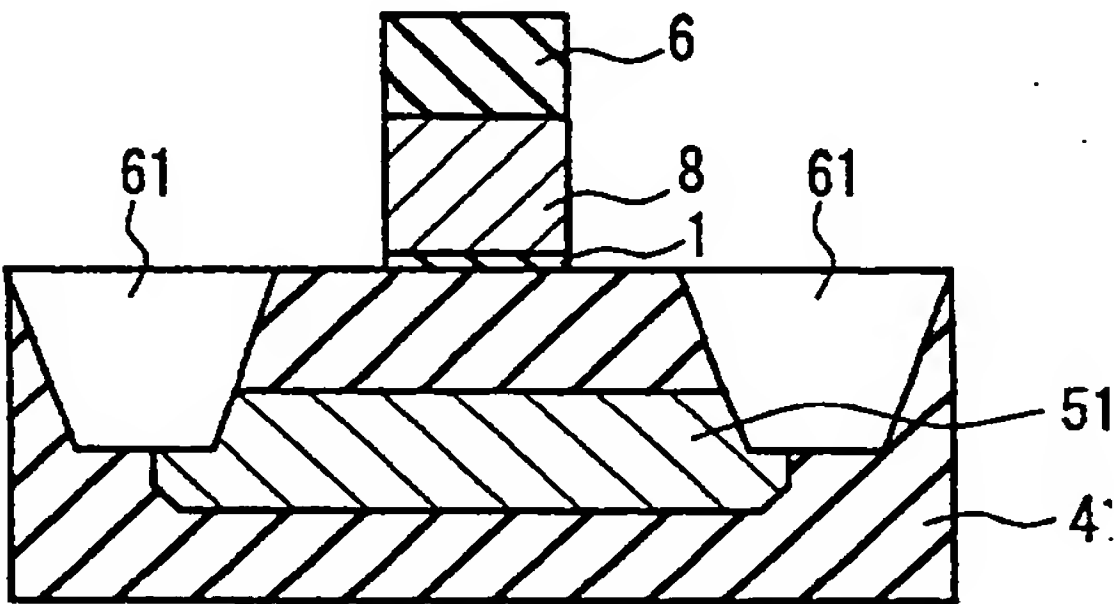


FIG. 1C

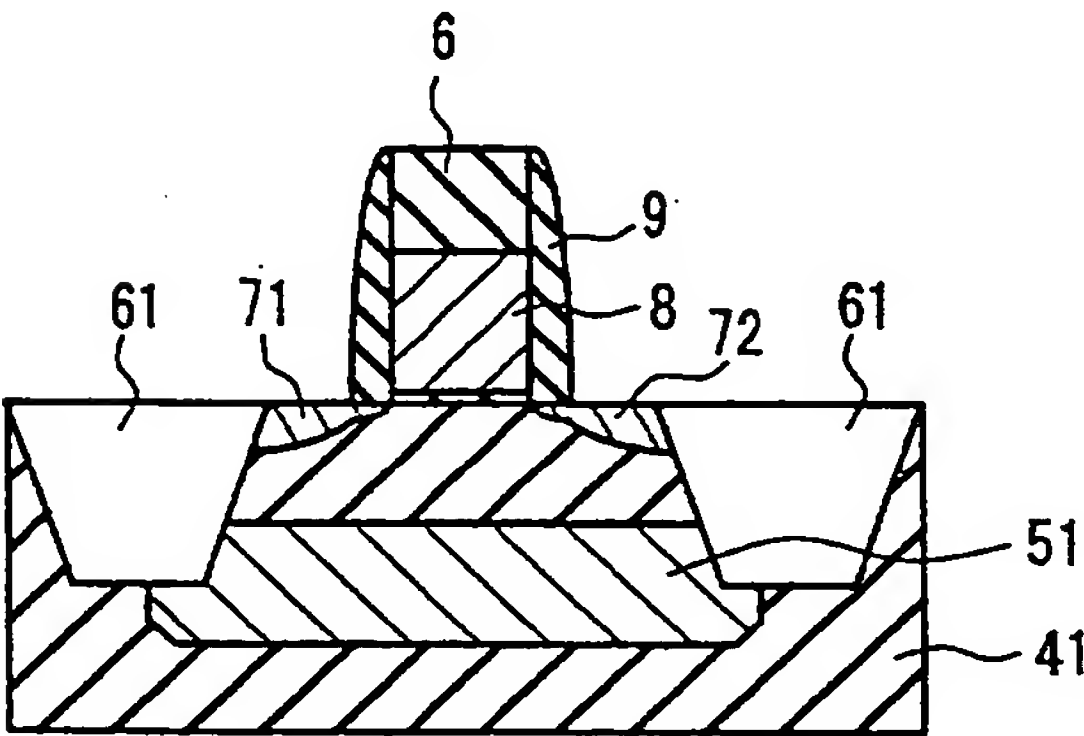


FIG. 1D

1

EP 1 347 503 A2

2

## Description

[0001] The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device. In particular, the present invention relates to a semiconductor device that includes a thin gate insulating film and a method for manufacturing the semiconductor device.

[0002] In LSIs (large scale integrated circuits), miniaturization of the elements, i.e., MOSFETs (metal oxide semiconductor field effect transistors) and a decrease in operating voltage have been pursued to increase the degree of integration per chip. With the achievement of highly integrated elements, a polymetal gate that uses a tungsten film instead of a tungsten silicide film for word lines has been studied to improve the speed of the elements. The specific resistance of the tungsten film is even lower than that of the tungsten silicide film.

[0003] For example, JP 11(1999)-261059 A discloses a method for fabricating a single p-channel MOS (metal oxide semiconductor) transistor that includes a polymetal gate with a conventional LP-SiN (low pressure chemical vapor deposition silicon nitride) film by using a STI (shallow trench isolation) process. FIGS. 9A to 9D are cross-sectional views showing the method in order. First, shallow trenches for isolation (STI) 161 are formed in a substrate 141, and then an n well 151 is formed by ion implantation of phosphorus (P) and arsenic (As) into a region between the trenches (FIG. 9A).

[0004] A RTP (rapid thermal process) is performed to form a gate insulating film 11 of an oxide film or oxynitride film. Using a LPCVD (low pressure chemical vapor deposition) chamber, an amorphous Si film 12 is grown in a  $\text{SiH}_4$  atmosphere, and then is doped with boron (B) by ion implantation. A titanium nitride (TiN) film 14 and a tungsten (W) film 15 are deposited in the order mentioned. A LP-SiN film 16 that serves as a gate-cap layer is formed on the tungsten film 15 in an atmosphere of  $\text{SiH}_2\text{Cl}_2$  (dichlorosilane, which may be abbreviated as "DCS" in the following) and  $\text{NH}_3$ . On top of that, a photoresist pattern 17 is formed to provide a gate pattern (FIG. 9B). The boron-implanted amorphous Si film 12, the titanium nitride film 14, and the tungsten film 15 constitute a gate electrode 18 in the subsequent process.

[0005] By using the photoresist pattern 17 as a mask, etching is performed to form a polymetal gate (gate electrode) 18 (FIG. 9C).

[0006] A side wall 19 is formed with the LP-SiN film. The side wall 19 is used to provide a LDD (lightly doped drain), a source ( $p^+$ ) 171, a drain ( $p^+$ ) 172, etc. (FIG. 9D).

[0007] For the polymetal gate thus produced, however, a large amount of hydrogen (H) is included in a range from the surface of the gate cap layer 16 to a depth of about 125 nm (FIG. 10). In FIG. 10, the horizontal axis indicates a depth (nm) from the surface of the LP-SiN film 16 (the gate cap layer) shown in FIG. 9D, and the vertical axis indicates the hydrogen concentration (atoms/ $\text{cm}^3$ ). The LP-SiN film 16 is formed of a  $\text{SiH}_2\text{Cl}_2$

gas including a Si-H bond and a  $\text{NH}_3$  gas including a N-H bond. Therefore, unreacted Si-H and N-H bonds remain in the silicon nitride film, so that a large amount of hydrogen (H) is entrapped. The unreacted Si-H and N-H bonds are separated by various heat treatments after the deposition of LP-SiN to generate hydrogen. This hydrogen diffuses into the gate insulating film and acts as an electron trap, causing a shift in the threshold voltage ( $V_{th}$ ) of a MOSFET and the degradation of an on-state current ( $I_{on}$ ).

[0008] Therefore, with the foregoing in mind, it is an object of the present invention to provide a semiconductor device that can suppress the diffusion of a large amount of hydrogen (H) into a gate insulating film and prevent a shift in the threshold voltage of a transistor and the degradation of an on-state current, and a method for manufacturing the semiconductor device.

[0009] A semiconductor device of the present invention includes a gate insulating film formed on a silicon substrate, a gate electrode formed on the gate insulating film, and an electrical insulating film formed on the gate electrode. The electrical insulating film includes a N-H bond and substantially no Si-H bond.

[0010] The electrical insulating film that includes substantially no Si-H bond is defined as not having a peak of Si-H stretching in a wave number range of 2100 to 2500  $\text{cm}^{-1}$  measured by a Fourier transform infrared spectrometer (FT-IR), or even if the film has the Si-H stretching peak, the peak is negligibly minute amount.

[0011] A method for manufacturing a semiconductor device includes forming a gate insulating film on a silicon substrate, forming a gate electrode on the gate insulating film, and forming an electrical insulating film on the gate electrode. The electrical insulating film is formed so as to include a N-H bond and substantially no Si-H bond by decomposition and deposition of a mixture of a gas including substantially no Si-H bond and a gas including a N-H bond.

[0012] These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

[0013] FIGS. 1A to 1D are cross-sectional views showing the processes of a method for manufacturing a semiconductor device of Embodiment 1 of the present invention.

[0014] FIG. 2 is a graph showing a hydrogen bond in silicon nitride films, which is measured by a Fourier transform infrared spectrometer (FT-IR). The silicon nitride films are produced respectively by a method of Embodiment 1 of the present invention and a conventional method.

[0015] FIG. 3 is a graph showing the hydrogen distribution of silicon nitride films having a polymetal gate structure, which is measured by a secondary ion mass spectrometer (SIMS). The silicon nitride films are produced respectively by a method of Embodiment 1 of the present invention and a conventional method.

[0016] FIG. 4 is a graph showing a shift in the threshold voltage ( $V_{th}$ ) of semiconductor devices that are manufactured respectively by a method of Embodiment 1 of the present invention and a conventional method.

[0017] FIGS. 5A to 5D are cross-sectional views showing the processes of a method for manufacturing a semiconductor device of Embodiment 2 of the present invention.

[0018] FIGS. 6A and 6B are graphs, each showing a hydrogen bond in silicon nitride films, which is measured by a FT-IR. The silicon nitride films are produced respectively by a method of Embodiment 2 of the present invention and a conventional method.

[0019] FIGS. 7A and 7B are graphs, each showing the hydrogen distribution of silicon nitride films having a polymetal gate structure, which is measured by a SIMS. The silicon nitride films are produced respectively by a method of Embodiment 2 of the present invention and a conventional method.

[0020] FIG. 8 is a graph showing a shift in the threshold voltage ( $V_{th}$ ) of semiconductor devices that are manufactured respectively by a method of Embodiment 2 of the present invention and a conventional method.

[0021] FIGS. 9A to 9D are cross-sectional views showing the processes of a method for manufacturing a conventional semiconductor device including a polymetal gate.

[0022] FIG. 10 is a graph showing the hydrogen distribution of a conventional silicon nitride film having a polymetal gate structure, which is measured by a SIMS.

[0023] In a semiconductor device of the present invention, an electrical insulating film (also referred to as "insulating film" in the following) is formed as a layer that includes a N-H bond and substantially no Si-H bond. The electrical insulating film is deposited on a gate electrode formed on a gate insulating film. The layer that includes a N-H bond and substantially no Si-H bond is, e.g., a silicon nitride film. Specifically, when analyzed by FT-IR measurement, the layer has a peak of N-H stretching in a wave number range of 3000 to 3500  $\text{cm}^{-1}$  and has no peak or a negligibly minute amount of peak of Si-H stretching in a wave number range of 2100 to 2500  $\text{cm}^{-1}$ .

[0024] It is preferable that the insulating film is a deposited film obtained by the decomposition of a mixture of a gas including substantially no Si-H bond and a gas including a N-H bond.

[0025] It is preferable that the gas including substantially no Si-H bond is a tetrachlorosilane gas, and the gas including a N-H bond is at least one gas selected from the group consisting of ammonia, dimethylamine, hydrazine, and dimethylhydrazine.

[0026] The thickness of the insulating film is preferably 50 nm to 300 nm, and more preferably 100 nm to 200 nm.

[0027] It is preferable that the gate electrode includes a polysilicon film implanted with boron ions, a metal film, or a laminated structure of a polysilicon film and a metal

film.

[0028] The present invention can provide a semiconductor device that uses an insulating film including substantially no Si-H bond (e.g., a silicon nitride film) as a cap film for a polymetal gate. Moreover, a gas including substantially no Si-H bond, e.g., tetrachlorosilane ( $\text{SiCl}_4$ , which may be abbreviated as "TCS" in the following) is used as a source gas for forming a silicon nitride film, thereby reducing a Si-H bond in the silicon nitride film. Thus, less hydrogen is separated by various heat treatments after the deposition of the silicon nitride film. Even if hydrogen diffuses into the gate insulating film, it is possible to prevent the insulating film (e.g., a silicon nitride film) from acting as an electron trap that causes a shift in the threshold voltage ( $V_{th}$ ) of a MOSFET and the degradation of a on-state current ( $I_{on}$ ).

[0029] A second method for manufacturing a semiconductor device of the present invention includes forming a gate insulating film on a silicon substrate, forming a gate electrode on the gate insulating film, and forming a silicon nitride film on the gate electrode by deposition of a source gas. The source gas may be a mixture of at least one gas selected from the group consisting of monosilane, dichlorosilane, and trichlorosilane and at least one gas selected from the group consisting of ammonia, dimethylamine, hydrazine, and dimethylhydrazine. It is preferable that the silicon nitride film is formed at temperatures of 750°C to 800°C.

[0030] In this manufacturing method, it is preferable that annealing is performed after the formation of the silicon nitride film so that the annealing temperature is higher than the temperature at which the silicon nitride film is formed.

[0031] A third method for manufacturing a third semiconductor device of the present invention includes forming a gate insulating film on a silicon substrate, forming a gate electrode on the gate insulating film, and forming a silicon nitride film on the gate electrode by deposition of a source gas. The source gas may be a mixture of at least one gas selected from the group consisting of monosilane, dichlorosilane, and trichlorosilane and at least one gas selected from the group consisting of ammonia, dimethylamine, hydrazine, and dimethylhydrazine. It is preferable that annealing is performed after the formation of the silicon nitride film so that the annealing temperature is higher than the temperature at which the silicon nitride film is formed.

[0032] It is preferable that the annealing temperature is 800°C to 1200°C, and that the annealing is performed in an atmosphere containing an inert gas, and further that the annealing is performed in an atmosphere of reduced pressure.

[0033] In the second and the third method, it is preferable that the gate electrode includes a polysilicon film implanted with boron ions, a metal film, or a laminated structure of a polysilicon film and a metal film.

[0034] The present invention allows annealing to be performed at temperatures higher than the deposition

temperature of a source gas. Therefore, even if dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) or the like is used as the source gas for forming a silicon nitride film (a cap film for a polymetal gate), an unreacted Si-H bond in the silicon nitride film is reduced. The annealing in an atmosphere of reduced pressure and a nitrogen gas or inert gas such as Ar particularly can reduce the unreacted Si-H bond. Thus, less hydrogen is separated by various heat treatments after the deposition of the silicon nitride film. This makes it possible to prevent hydrogen from diffusing into the gate insulating film, acting as an electron trap, and causing a shift in the threshold voltage ( $V_{th}$ ) of a MOSFET and the degradation of a on-state current ( $I_{on}$ ).

[0035] The present invention can provide a semiconductor device that is provided with a gate cap insulating film including substantially no Si-H bond or a semiconductor device that uses a silicon nitride film including fewer Si-H and N-H bonds as a gate gap insulating film. Therefore, the diffusion of hydrogen into the polymetal gate electrode and the gate insulating film can be suppressed to prevent a shift in the threshold voltage of a transistor and the degradation of an on-state current.

[0036] Hereinafter, specific embodiments of the present invention will be described with reference to the drawings.

#### Embodiment 1

[0037] FIGS. 1A to 1D are cross-sectional views showing processes for forming a gate cap insulating film of a semiconductor device in order, according to Embodiment 1 of the present invention. FIGS. 1A to 1D illustrate an example of the fabrication of a single n-channel MOS transistor on a p-type silicon substrate using a STI process. Instead of the STI process, e.g., LOCOS (local oxidation of silicon) may be employed to form a region for isolating elements.

[0038] First, shallow trenches for isolation (STI) 61 are formed in a silicon substrate 41. The trenches 61 are produced by dry etching. Then, an n well 51 is formed by ion implantation of phosphorus (P) and arsenic (As) into a region between the trenches (FIG. 1A).

[0039] A RTP (rapid thermal process) is performed in an atmosphere of oxygen or nitrogen to form a gate insulating film 1 having a thickness of about 2.5 nm. The gate insulating film 1 is made of an oxide film or oxynitride film.

[0040] Using a LPCVD chamber, an amorphous Si film 2 is grown to have a thickness of about 80 nm in a  $\text{SiH}_4$  atmosphere, which then is doped with boron (B) by ion implantation. A titanium nitride (TiN) film 4 having a thickness of about 10 nm and a tungsten (W) film 5 having a thickness of about 50 nm are deposited in the order mentioned. ALP-SiN film 6 (a gate cap layer) having a thickness of about 150 nm is formed on the tungsten film 5 in a mixed atmosphere of tetrachlorosilane ( $\text{SiCl}_4$ ) and ammonia ( $\text{NH}_3$ ) at 760°C.

[0041] A photoresist pattern 7 is formed to provide a

gate pattern (FIG. 1B). The boron-implanted amorphous Si film 2, the titanium nitride (TiN) film 4, and the tungsten (W) film 5 constitute a gate electrode 8 in the subsequent process.

5 [0042] By using the photoresist pattern 7 as a mask, etching is performed to form a polymetal gate (gate electrode) 8 (FIG. 1C).

[0043] Next, a side wall 9 having a thickness of about 120 nm is formed with the LP-SiN film. The side wall 9 is used to provide a LDD (lightly doped drain) structure, a source ( $p^+$ ) 71, and a drain ( $p^+$ ) 72, etc. (FIG. 1D).

10 [0044] The temperature at which the LP-SiN film 6 is formed ranges from 500°C to 800°C, and preferably 700°C to 800°C. Temperatures of not less than 500°C can reduce hydrogen in the silicon nitride film, and temperatures of not more than 800°C can ensure the heat resistance of the gate electrode.

15 [0045] In this embodiment, a gas mixture of tetrachlorosilane and ammonia is used as a source gas for forming the film. The source gas is not particularly limited as long as it includes substantially no Si-H bond, and can be a mixture of a tetrachlorosilane gas and a gas including a N-H bond. The deposition of this source gas results in a silicon nitride film that includes substantially no Si-H bond.

20 [0046] The gas including a N-H bond can be, e.g., ammonia, lower amine such as monomethylamine ( $\text{NH}_2\text{CH}_3$ ), hydrazine ( $\text{N}_2\text{H}_4$ ), and a derivative of these compounds such as dimethylamine ( $\text{NH}(\text{CH}_3)_2$ ) and dimethylhydrazine ( $\text{CH}_3\text{NHNHCH}_3$ ).

25 [0047] The LP-SiN films 6 were produced respectively by a method of this embodiment and a conventional method. Then, a hydrogen bond in each of the silicon nitride films was measured by a Fourier transform infrared spectrometer (FT-IR). FIG. 2 is a graph showing the results. The horizontal axis indicates the wave numbers, and the vertical axis indicates the absorbance. The silicon nitride film 6 of the present invention used a source gas of TCS ( $\text{SiCl}_4$ ), while the conventional film used a source gas of DCS ( $\text{SiH}_2\text{Cl}_2$ ). As shown in FIG. 2, both the silicon nitride films 6 of the present invention and the conventional example had a peak of N-H stretching (ranging from 3000 to 3500  $\text{cm}^{-1}$ ). However, only the conventional film formed of DCS had a peak of Si-H stretching (ranging from 2100 to 2500  $\text{cm}^{-1}$ ). Compared with DCS ( $\text{SiH}_2\text{Cl}_2$ ) and TCS ( $\text{SiCl}_4$ ), this is attributed to a Si-H bond in the molecular structure of DCS. Moreover, the bond energy of the Si-H bond is lower than that of the N-H bond, and thus the Si-H bond breaks easily. Consequently, the hydrogen separated from the Si-H bond may diffuse into the gate insulating film 1, causing a shift in the threshold voltage ( $V_{th}$ ) and the degradation of an on-state current ( $I_{on}$ ).

30 [0048] FIG. 3 is a graph showing the hydrogen distribution of the LP-SiN films 6 having a polymetal gate structure, which were produced respectively by a method of this embodiment and a conventional method. The horizontal axis indicates a depth (nm) from the surface

7

EP 1 347 503 A2

8

of the LP-SiN film 6, and the vertical axis indicates the hydrogen concentration (atoms/cm<sup>3</sup>). The hydrogen concentration was measured by a secondary ion mass spectrometer (SIMS).

[0049] As shown in FIG. 3, the amount of hydrogen (H) in the vicinity of the interface between the gate insulating film 1 and the polycrystalline gate electrode 8 (i.e., the portion indicated by Gox in FIG. 3) is made smaller for this embodiment (using a source gas of TCS) than for the conventional example (using a source gas of DCS). This result shows that hydrogen that has been separated from the Si-H bond diffuses into the gate insulating film 1.

[0050] FIG. 4 is a graph showing a shift in the threshold voltage (V<sub>th</sub>) of semiconductor devices, which were manufactured respectively by a method of this embodiment (a source gas: TCS, and a film forming temperature: 760°C) and a conventional method (a source gas: DCS, and a film forming temperature: 700°C). The horizontal axis indicates the type of source gas, and the vertical axis indicates the amount of shift in V<sub>th</sub>. FIG. 4 shows that the silicon nitride film of this embodiment can suppress a shift in the threshold voltage (V<sub>th</sub>).

[0051] The silicon nitride film (Si<sub>3</sub>N<sub>4</sub>) 6 formed according to this embodiment as an insulating film on the polycrystalline gate 8 can suppress a shift in the threshold voltage (V<sub>th</sub>), which has been prominent in a conventional silicon nitride film. This is because the amount of hydrogen in the film can be reduced by using a gas that contains no hydrogen, i.e., tetrachlorosilane (SiCl<sub>4</sub>), thus eliminating the cause of an electron trap. Moreover, hydrogen (H) usually is joined to a dangling bond generated in the manufacturing process of a semiconductor. In this embodiment, however, the dangling bond can be terminated by halogen such as chlorine (Cl) instead of hydrogen (H).

[0052] As described above, the silicon nitride film 6 of this embodiment is formed by using tetrachlorosilane (SiCl<sub>4</sub>) as a source gas, thereby effectively preventing the diffusion of hydrogen (H) into the gate insulating film.

#### Embodiment 2

[0053] FIGS. 5A to 5D are cross-sectional views showing processes for forming a gate cap insulating film of a semiconductor device in order, according to Embodiment 2 of the present invention. FIGS. 5A to 5D illustrate an example of the fabrication of a single n-channel MOS transistor on a p-type silicon substrate using a STI process. Instead of the STI process, e.g., LOCOS may be employed to form a region for isolating elements.

[0054] First, like FIG. 1A, shallow trenches for isolation (STI) 61 are formed, and then an n well 51 is formed by ion implantation of phosphorous (P) and arsenic (As) into a region between the trenches (FIG. 5A).

[0055] A RTP (rapid thermal process) is performed to form a gate insulating film 1 of an oxide film or oxynitride

film. Using a LPCVD chamber, an amorphous Si film 2 is grown in a SiH<sub>4</sub> atmosphere, which then is doped with boron (B) by ion implantation. A titanium nitride (TiN) film 4 and a tungsten (W) film 5 are deposited in the order mentioned. A LP-SiN film 31 (a gate-cap layer) is formed on the tungsten film 5 in a mixed atmosphere of dichlorosilane (SiH<sub>2</sub>Cl<sub>2</sub>) and ammonia (NH<sub>3</sub>) at 700° (in a conventional method) or 760°C. The silicon nitride film 31 is annealed for 60 minutes under the conditions of a nitrogen atmosphere, 10<sup>2</sup> to 10<sup>5</sup> Pa, and 800°C. Subsequently, a photoresist pattern 7 is formed to provide a gate pattern (FIG. 5B).

[0056] By using the photoresist pattern 7 as a mask, etching is performed to form a polycrystalline gate 8 (FIG. 5C).

[0057] Next, a side wall 9 is formed with the LP-SiN film 31. The side wall 9 is used to provide a LDD (lightly doped drain) structure, a source (p<sup>+</sup>) 71, a drain (p<sup>+</sup>) 72, etc. (FIG. 5D).

[0058] The temperature at which the LP-SiN film 31 is formed ranges from 500°C to 800°C, preferably 700°C to 800°C, and more preferably 750°C to 800°C. Temperatures of not less than 700°C can reduce the residual hydrogen in the silicon nitride film, and temperatures of not more than 800°C can ensure the heat resistance of the gate electrode.

[0059] In this embodiment, a gas mixture of dichlorosilane and ammonia is used as a source gas for forming the film. The dichlorosilane may be replaced, e.g., by monosilane, trichlorosilane, etc. Thus, the source gas can be a mixture of the above silane gas and a gas including a N-H bond.

[0060] The gas including a N-H bond can be, e.g., ammonia, lower amine such as monomethylamine (NH<sub>2</sub>CH<sub>3</sub>), hydrazine (N<sub>2</sub>H<sub>4</sub>), and a derivative of these compounds such as dimethylamine (NH(CH<sub>3</sub>)<sub>2</sub>) and dimethylhydrazine (CH<sub>3</sub>NHNHCH<sub>3</sub>).

[0061] The annealing temperature is higher than the temperature at which the silicon nitride film is formed, and desirably not less than 800°C. The annealing temperature of not less than 800°C can eliminate the residual hydrogen in the silicon nitride film. It is preferable that the annealing temperature is not more than 1200°C in view of the heat resistance of the gate electrode. The annealing time generally is 5 to 120 minutes, and preferably 30 to 60 minutes. Considering the film characteristics of the silicon nitride film, the annealing should be performed in an inert gas atmosphere. Examples of the inert gas include a low reactive gas such as a nitrogen gas and a rare gas such as Ar. Although the annealing can be performed at atmospheric pressure or reduced pressure, an atmosphere of reduced pressure is preferred for reducing an unreacted Si-H bond.

[0062] The LP-SiN films 31 were produced respectively by a method of this embodiment and a conventional method. Then, a hydrogen bond in each of the silicon nitride films was measured by a FT-IR. FIGS. 6A and 6B are graphs showing the results. The horizontal

9

EP 1 347 503 A2

10

axis indicates the wave numbers, and the vertical axis indicates the absorbance. In FIG. 6A, both the silicon nitride films of this embodiment and the conventional example were formed by depositing DCS at 700°C. However, they differed in subsequent process, that is, the silicon nitride film of this embodiment was annealed in a nitrogen atmosphere at 800°C for 60 minutes, while the conventional film was not annealed. In FIG. 6B, the silicon nitride film of this embodiment was formed by depositing DCS at 760°C, and the conventional film was formed by depositing DCS at 700°C. In this case, neither of the silicon nitride films was annealed.

[0063] As shown in FIG. 6A, the peak of N-H stretching (ranging from 3000 to 3500  $\text{cm}^{-1}$ ) and the peak of Si-H stretching (ranging from 2100 to 2500  $\text{cm}^{-1}$ ) of the silicon nitride film that has been annealed at temperatures higher than the film forming temperature are made lower than those of the unannealed film.

[0064] As shown in FIG. 6B, the peak of N-H stretching (ranging from 3000 to 3500  $\text{cm}^{-1}$ ) and the peak of Si-H stretching (ranging from 2100 to 2500  $\text{cm}^{-1}$ ) are higher than those shown in FIG. 6A. These results show that the N-H bond and the Si-H bond are reduced by forming the silicon nitride film at higher temperatures. The reason for this is considered to be as follows: the film forming temperature is increased from 700°C (the conventional example) to 760°C, and the annealing is performed at temperatures (800°C) higher than the film forming temperature, so that the residual Si-H and N-H bonds in the silicon nitride film are broken to cause the diffusion of hydrogen from the silicon nitride film.

[0065] FIGS. 7A to 7B are graphs showing the hydrogen distribution of the LP-SiN films 31 having a polymetal gate structure, which were produced respectively by a method of this embodiment and a conventional method. The horizontal axis indicates a depth (nm) from the surface of the LP-SiN film 31, and the vertical axis indicates hydrogen concentration (atoms/ $\text{cm}^3$ ). The hydrogen concentration was measured by a SIMS.

[0066] In FIG. 7A, both the silicon nitride films of this embodiment and the conventional example were formed by depositing DCS at 700°C. However, they differed in subsequent process, that is, the silicon nitride film of this embodiment was annealed in a nitrogen atmosphere at 800°C, while the conventional film was not annealed. In FIG. 7B, the silicon nitride film of this embodiment was formed by depositing DCS at 760°C, and the conventional film was formed by depositing DCS at 700°C. In this case, neither of the silicon nitride films was annealed.

[0067] As shown in FIG. 7A, the amount of hydrogen (H) in the vicinity of the interface between the gate insulating film 1 and the polymetal gate electrode 8 is reduced by annealing the silicon nitride film at temperatures (e.g., 800°C) higher than the film forming temperature when compared to the unannealed film.

[0068] As shown in FIG. 7B, the amount of hydrogen (H) in the vicinity of the interface between the gate in-

sulating film 1 and the polymetal gate electrode 8 is reduced by increasing the film forming temperature from 700°C (the conventional example) to 760°C.

[0069] FIG. 8 is a graph showing a shift in the threshold voltage ( $V_{th}$ ) of semiconductor devices, which were manufactured respectively by a method of this embodiment (a film forming temperature: 700°C, and annealing at 800°C for 60 min.), a first comparative method (a film forming temperature: 700°C, and without annealing), and a second comparative method (a film forming temperature: 700°C, and annealing at 700°C for 60 min.). The horizontal axis indicates the conditions of annealing, and the vertical axis indicates the amount of shift in  $V_{th}$ . FIG. 8 shows that the silicon nitride film that is annealed at 800°C can suppress a shift in the threshold voltage ( $V_{th}$ ).

[0070] The silicon nitride film ( $\text{Si}_3\text{N}_4$ ) 31 formed according to this embodiment as an insulating film on the polymetal gate 8 can suppress a shift in the threshold voltage ( $V_{th}$ ), which has been prominent in a conventional silicon nitride film. This is because the amount of hydrogen in the film can be reduced by increasing the film forming temperature compared with the conventional method and annealing the silicon nitride film desirably at temperatures higher than the film forming temperature, thus eliminating the cause of an electron trap.

## Claims

1. A semiconductor device comprising:

a gate insulating film formed on a silicon substrate;  
a gate electrode formed on the gate insulating film; and  
an electrical insulating film formed on the gate electrode,

wherein the electrical insulating film includes a N-H bond and substantially no Si-H bond.

2. The semiconductor device according to claim 1, wherein the electrical insulating film is a silicon nitride film.

3. The semiconductor device according to claim 1, wherein the gate electrode comprises a polysilicon film implanted with boron ions, a metal film, or a laminated structure of a polysilicon film and a metal film.

4. A method for manufacturing the semiconductor device according to any one of claims 1 to 3 comprising:

forming the electrical insulating film that includes a N-H bond and substantially no Si-H bond by decomposition and deposition of a mix-

ture of a gas including substantially no Si-H bond and a gas including a N-H bond.

- 5. The method according to claim 4, wherein the electrical insulating film is a silicon nitride film. 5
  
- 6. The method according to claim 4, wherein the gas mixture comprises a tetrachlorosilane gas and a gas including a N-H bond. 10
  
- 7. The method according to claim 4, wherein the gas including a N-H bond is at least one gas selected from the group consisting of ammonia, dimethylamine, hydrazine, and dimethylhydrazine. 15
  
- 8. A method for manufacturing the semiconductor device according to any one of claims 1 to 3 comprising:  
  
forming the electrical insulating film by using a gas mixture as a source gas to form a silicon nitride film at temperatures of 750°C to 800°C, the gas mixture comprising at least one gas selected from the group consisting of monosilane, dichlorosilane, and trichlorosilane and at least one gas selected from the group consisting of ammonia, dimethylamine, hydrazine, and dimethylhydrazine as a gas including a N-H bond. 20 25 30
  
- 9. The method according to claim 8, wherein annealing is performed after the formation of the silicon nitride film so that an annealing temperature is higher than a temperature at which the silicon nitride film is formed. 35
  
- 10. The method according to claim 9, wherein the annealing temperature is 800°C to 1200°C.
  
- 11. The method according to claim 9, wherein the annealing is performed in an atmosphere containing an inert gas. 40
  
- 12. The method according to claim 9, wherein the annealing is performed in an atmosphere of reduced pressure. 45

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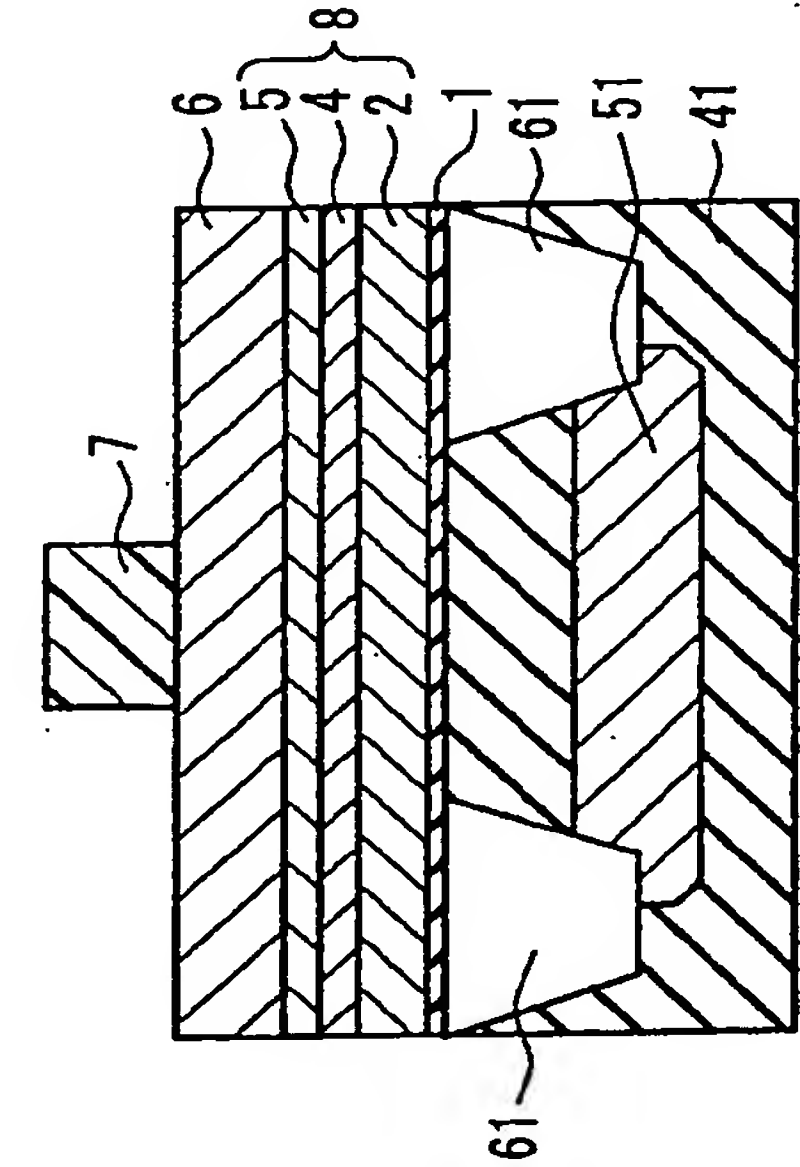


FIG. 1A

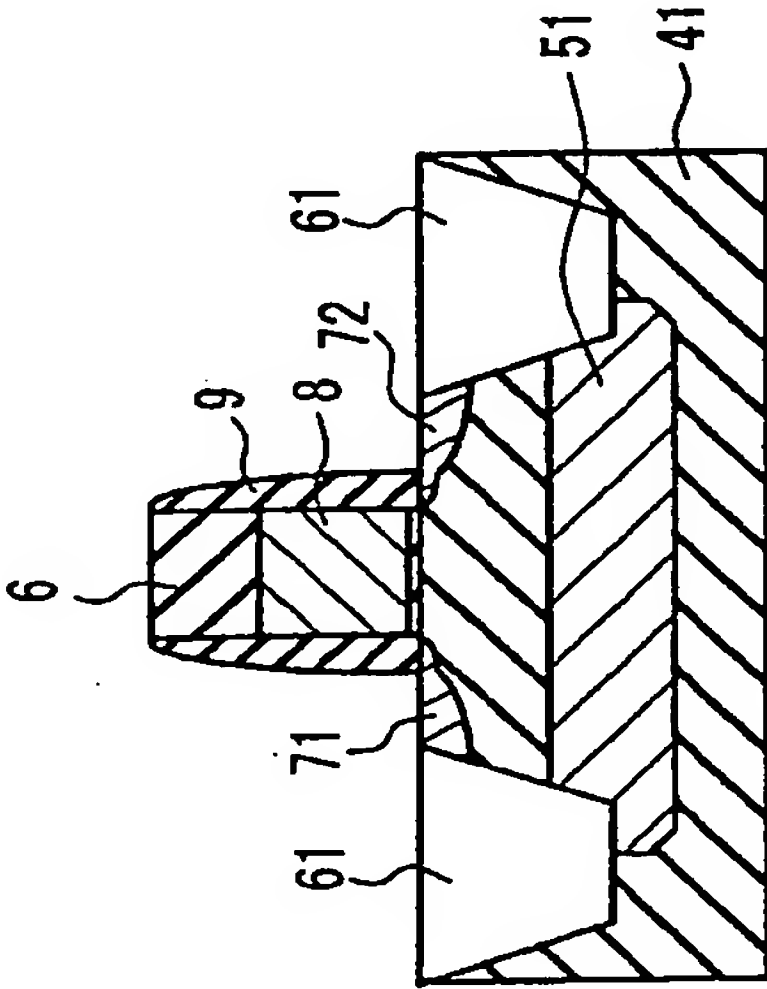


FIG. 1B

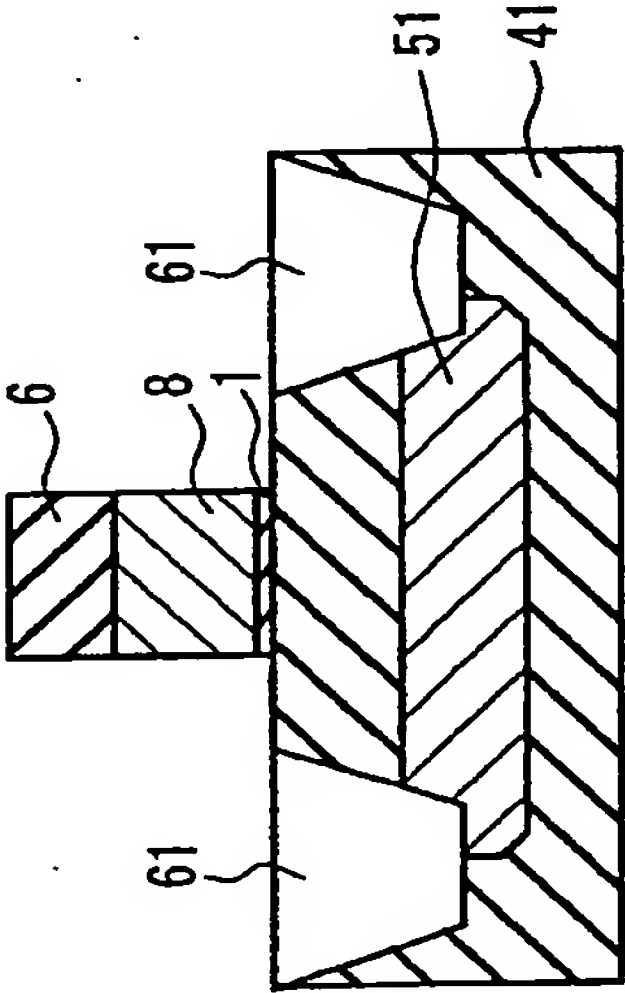


FIG. 1C

FIG. 1D

EP 1 347 503 A2

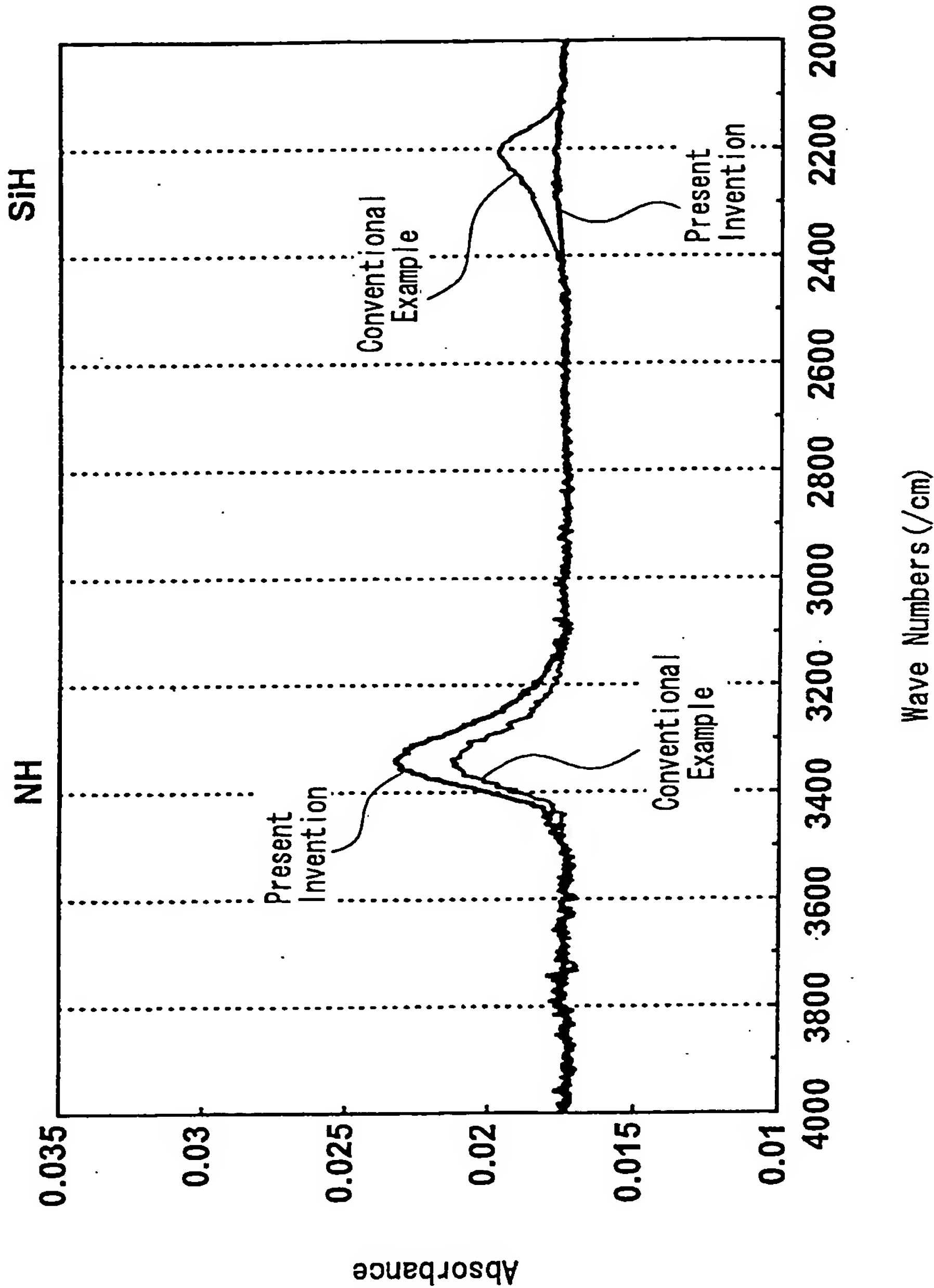


FIG. 2

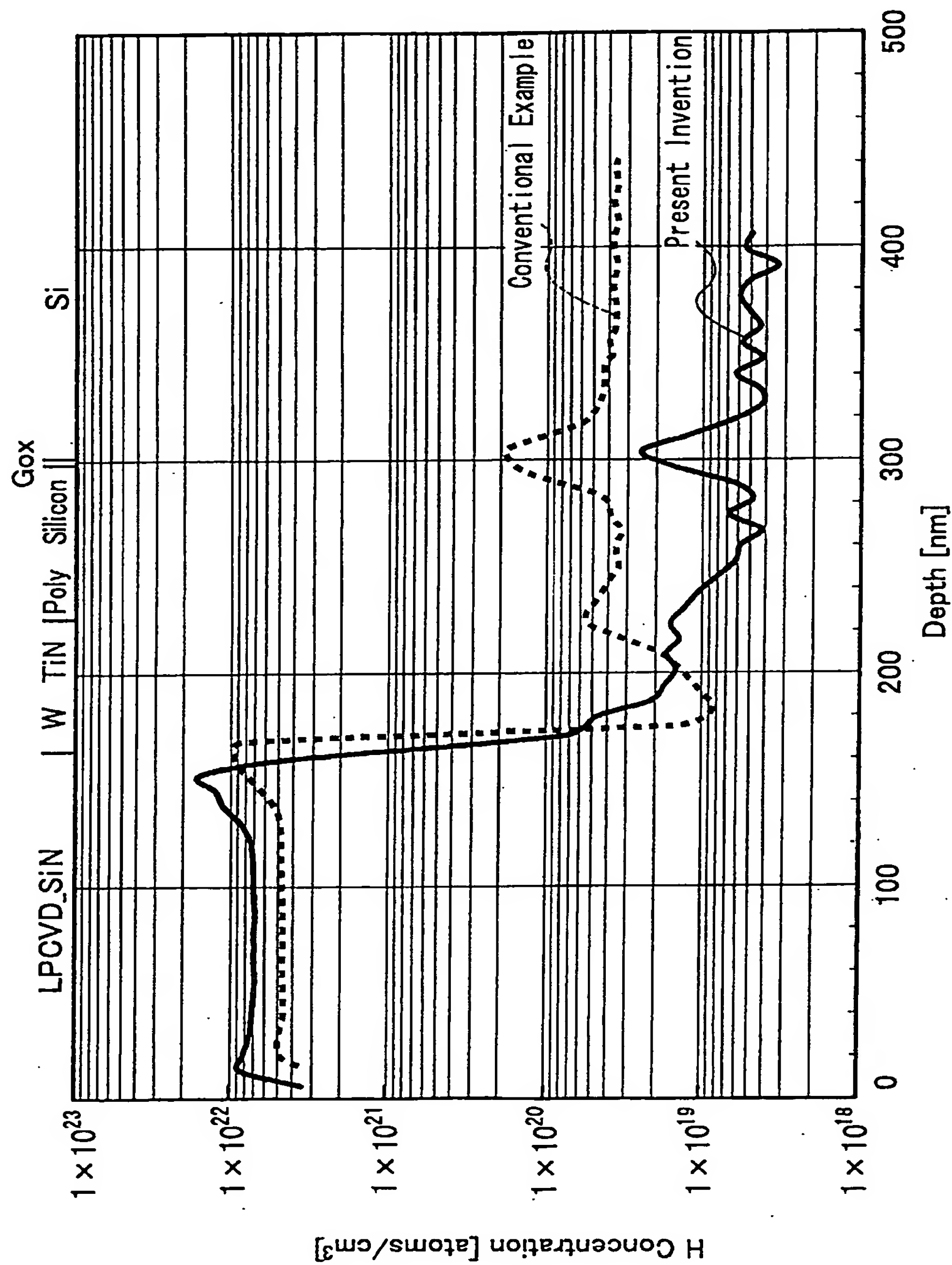


FIG. 3

EP 1 347 503 A2

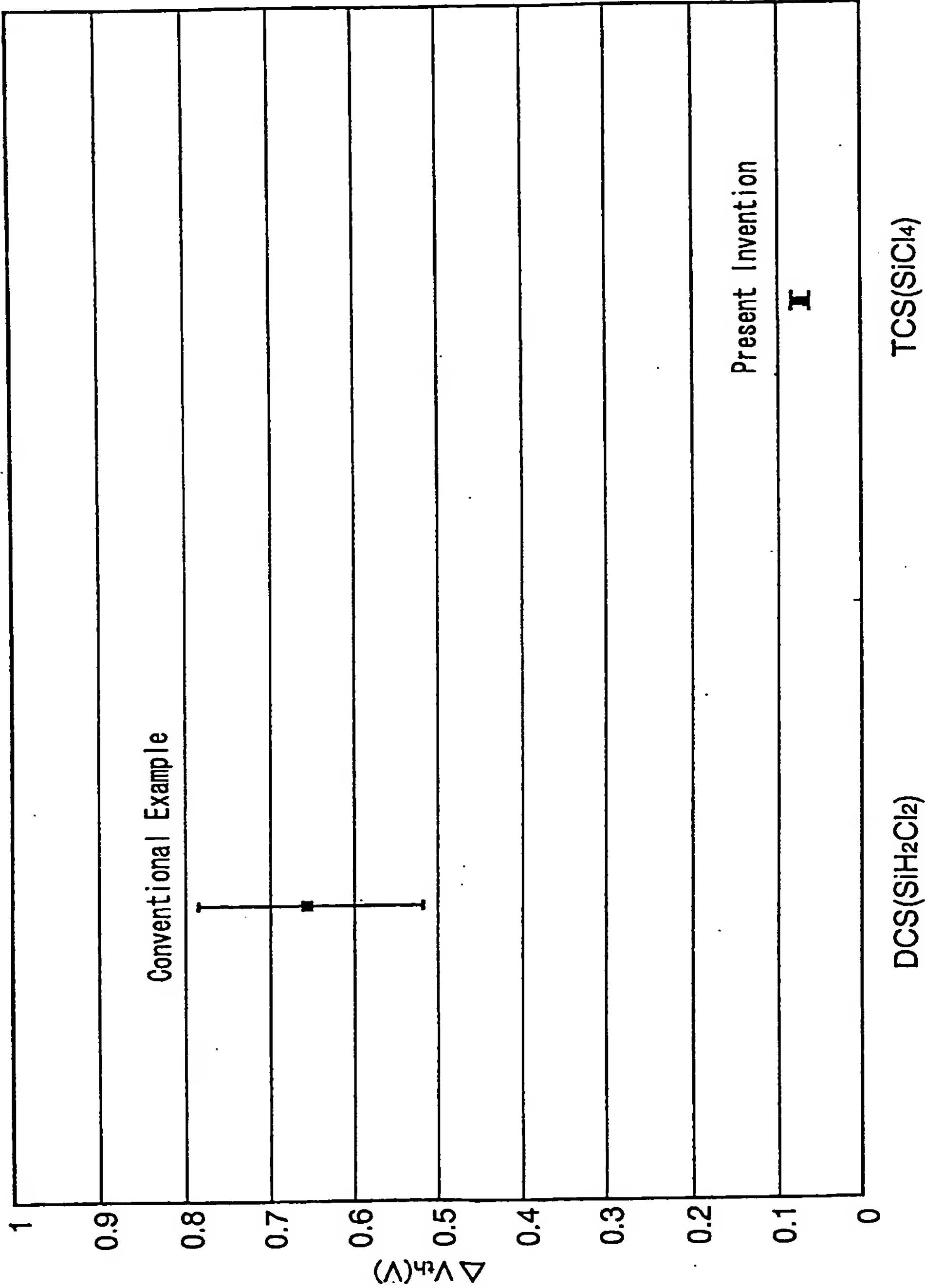


FIG. 4

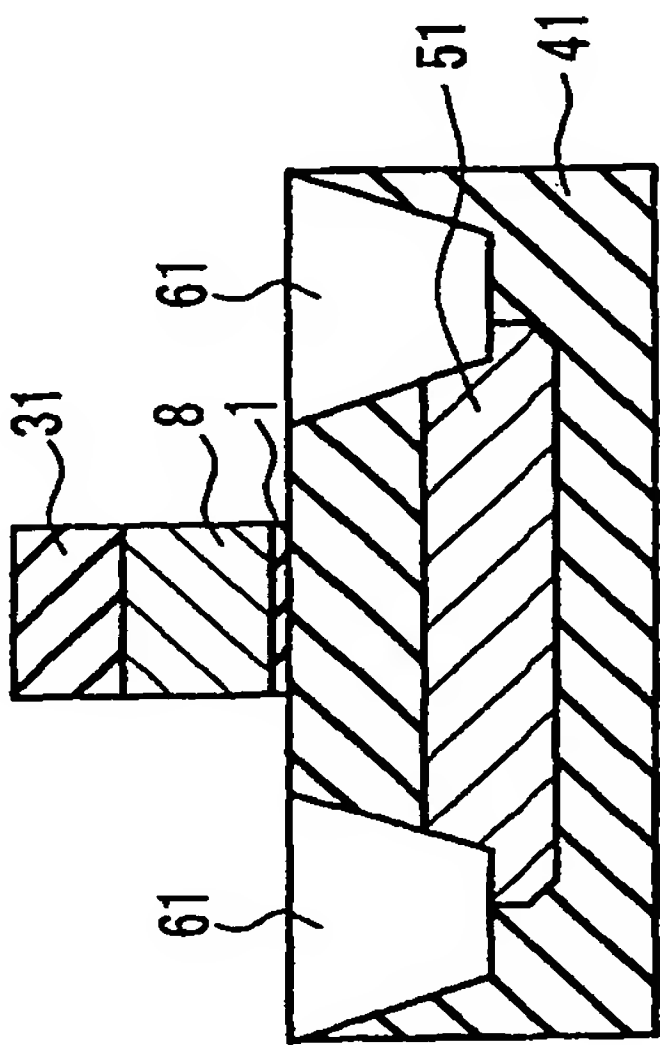


FIG. 5C

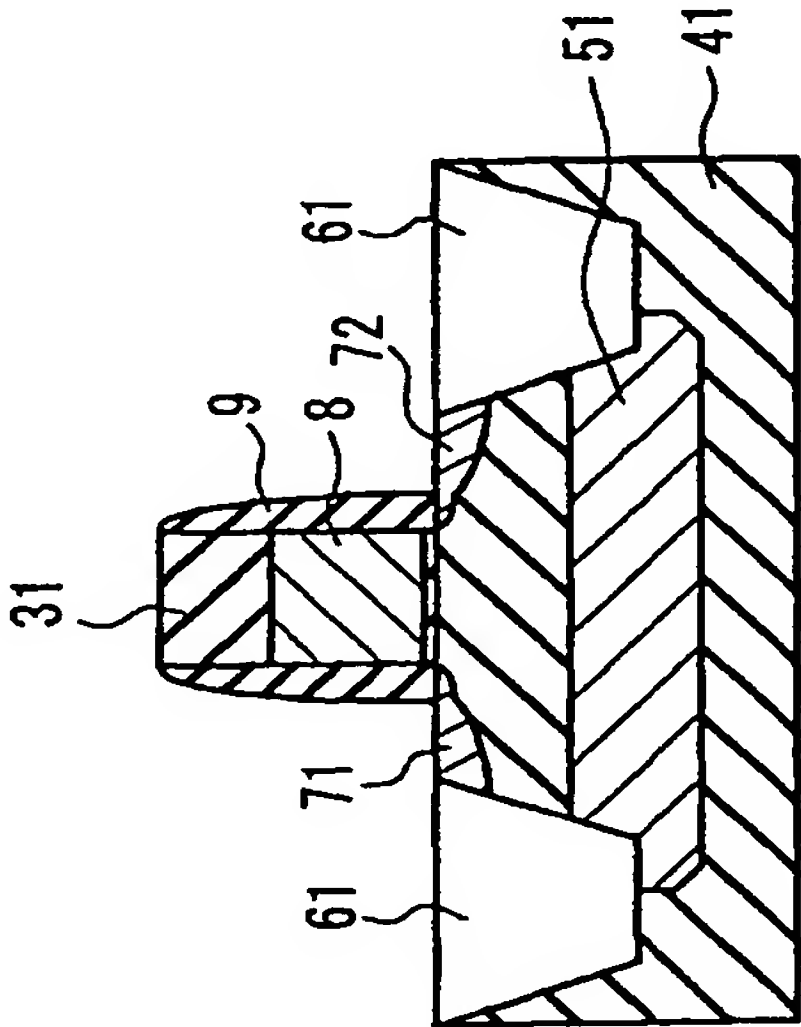


FIG. 5D

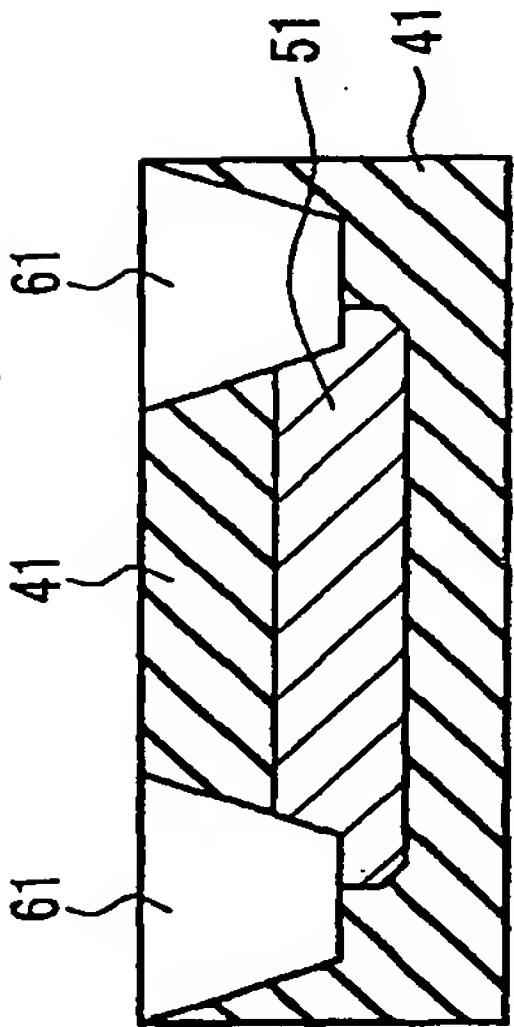


FIG. 5A

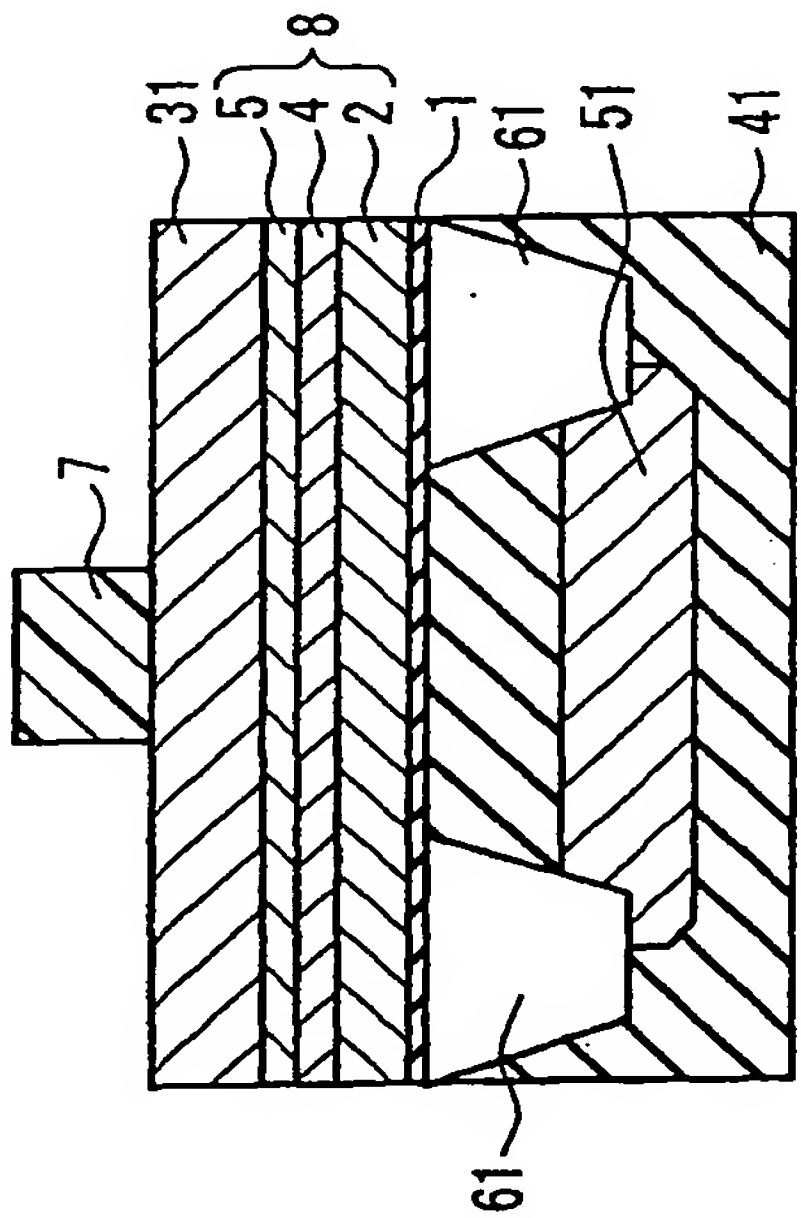


FIG. 5B

EP 1 347 503 A2

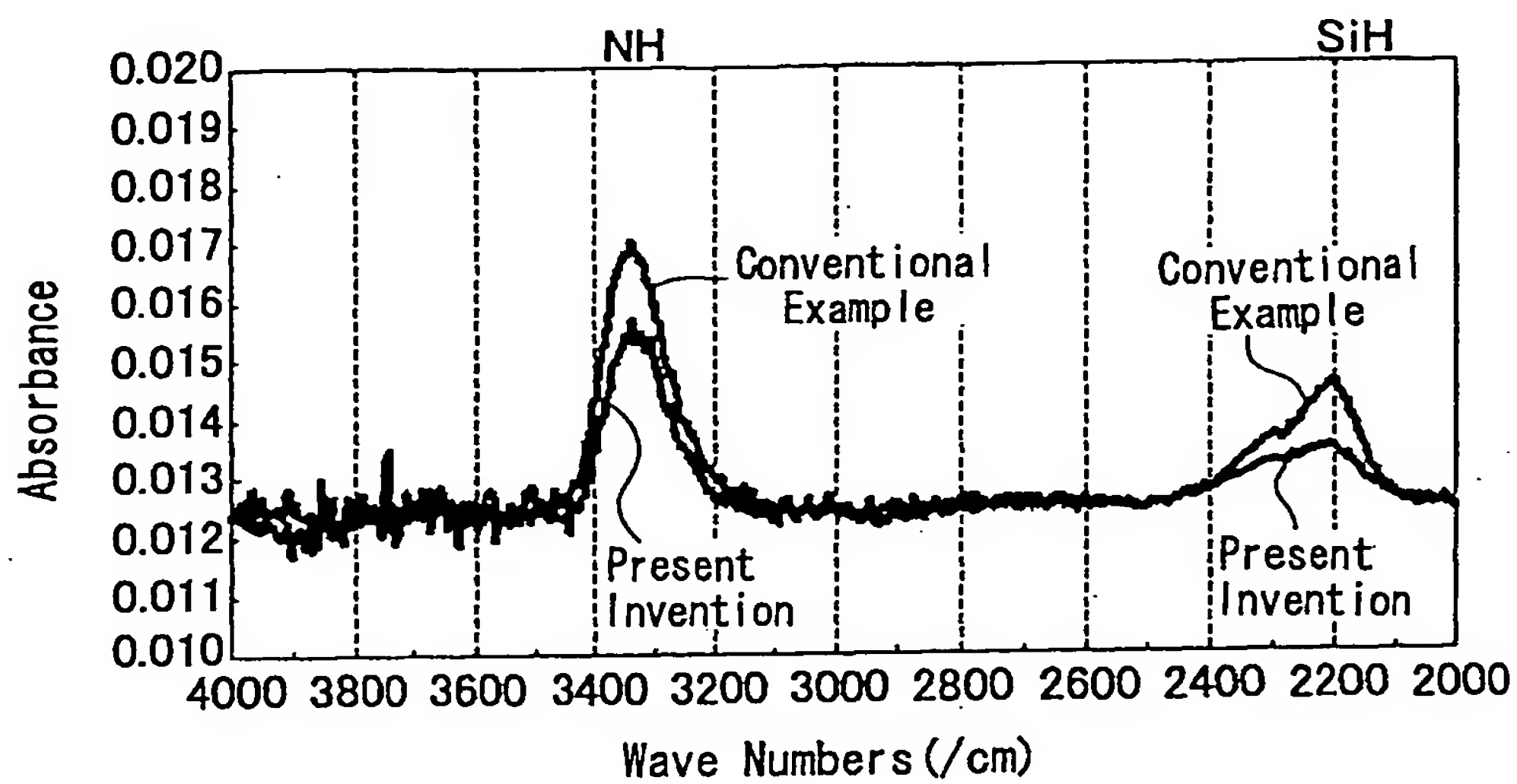


FIG. 6A

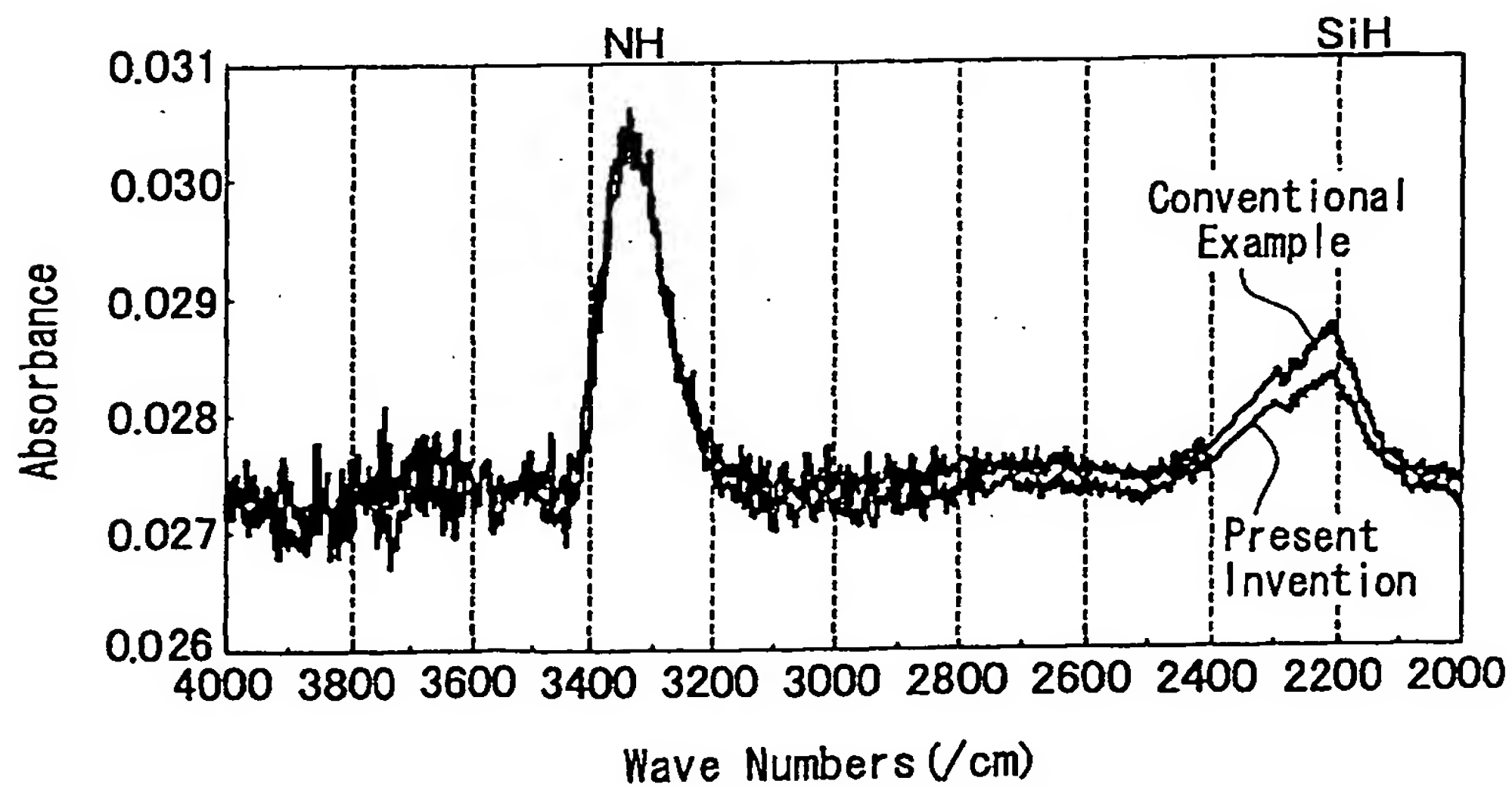


FIG. 6B

EP 1 347 503 A2

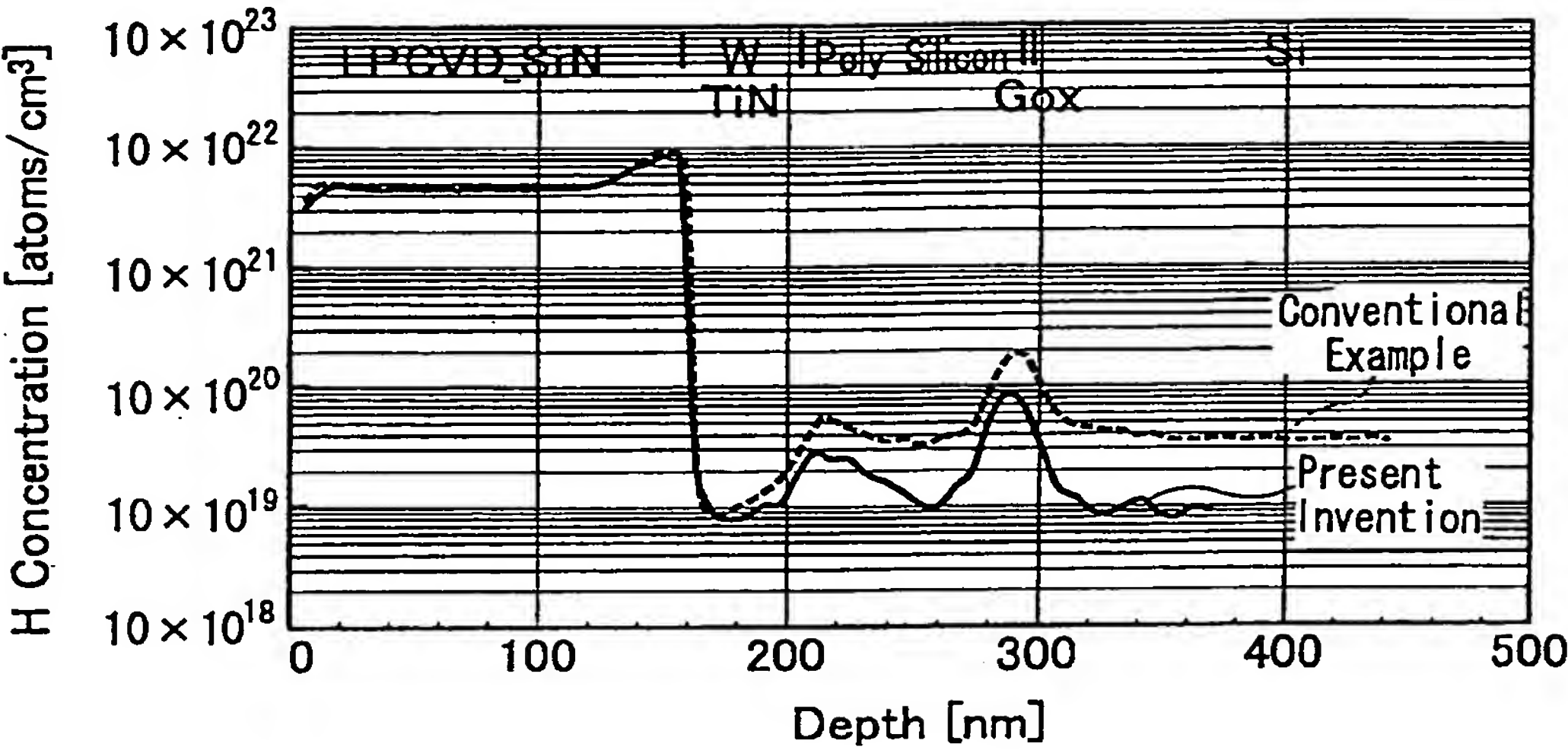


FIG. 7A

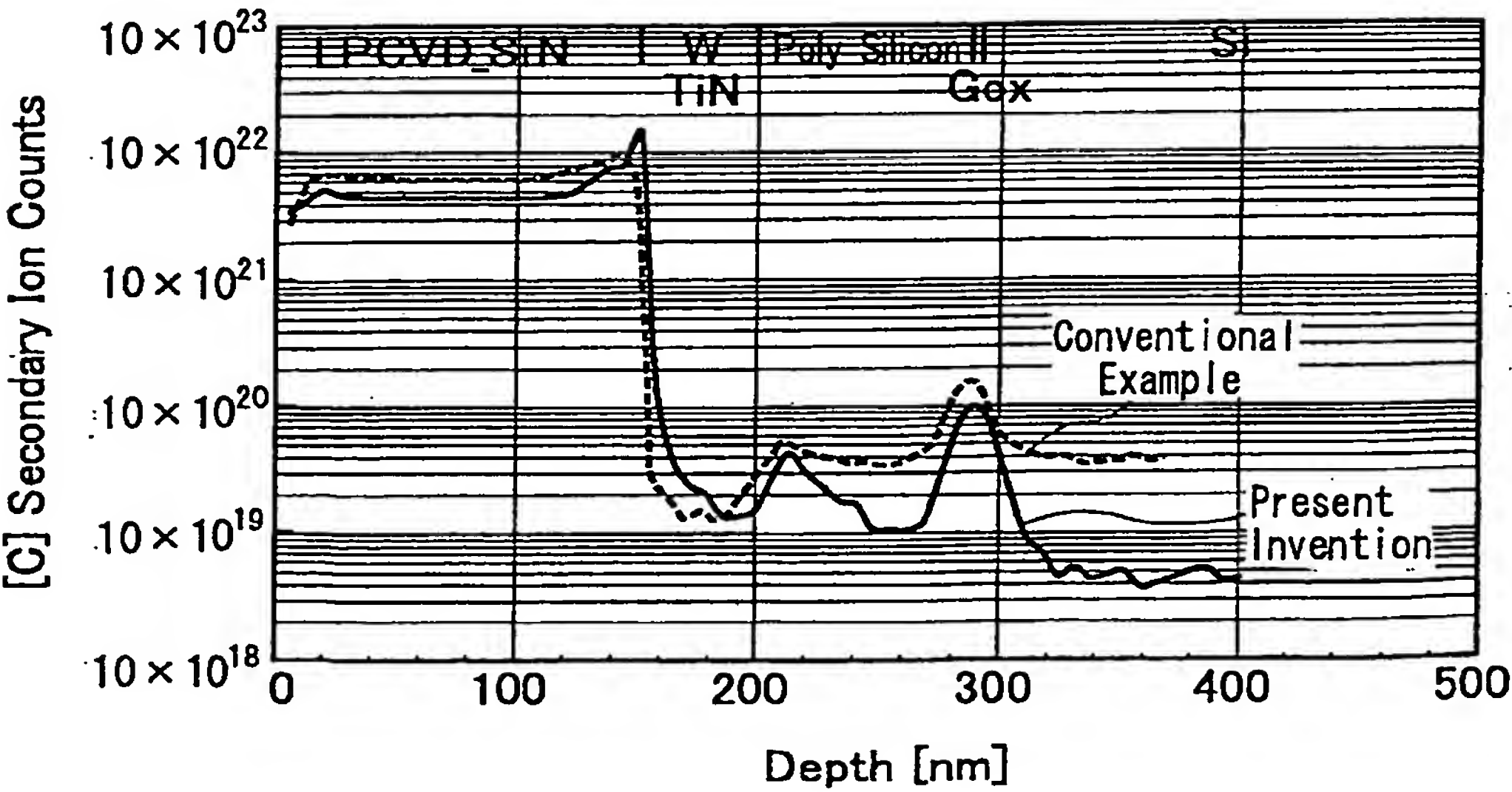


FIG. 7B

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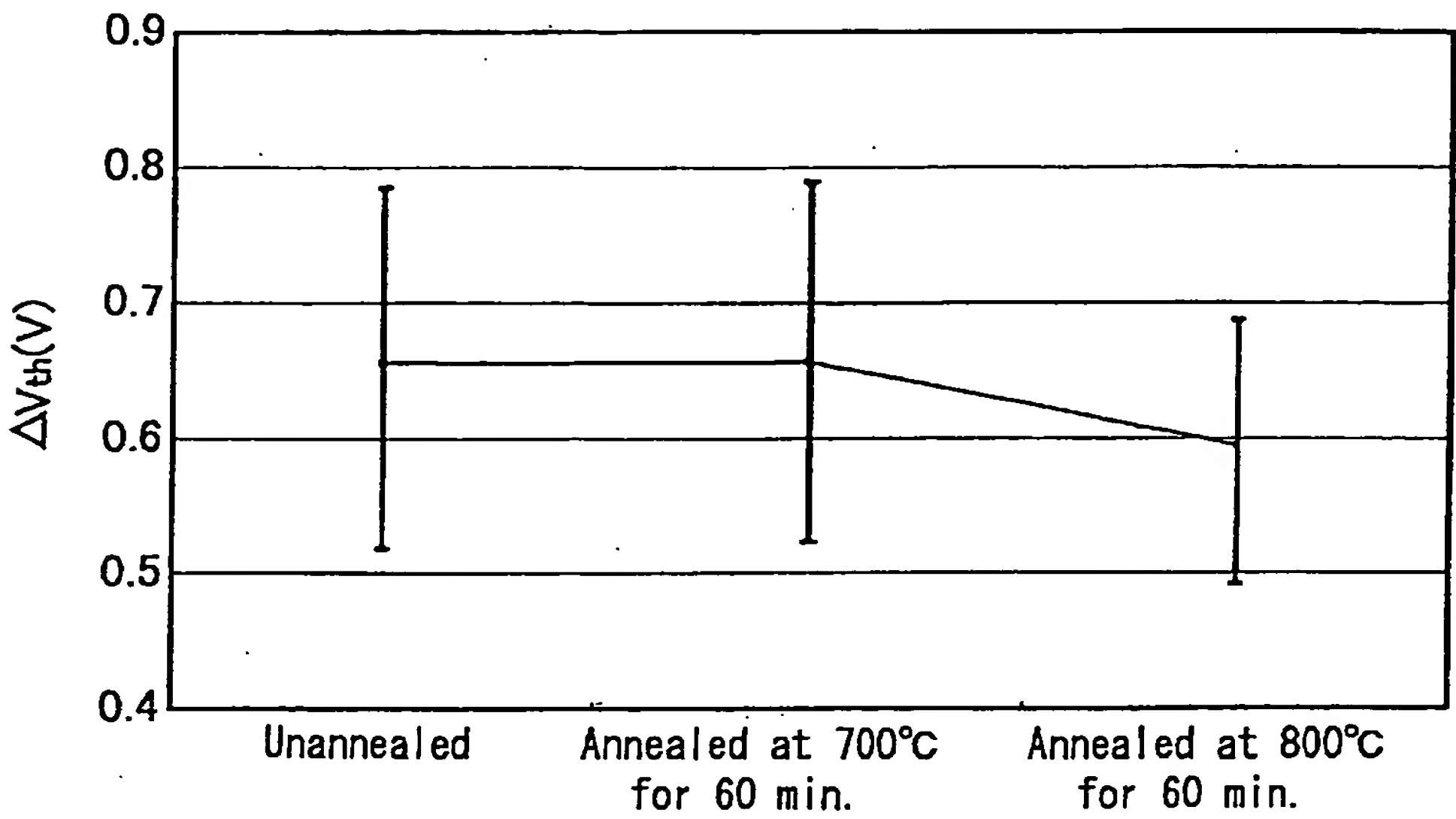


FIG. 8

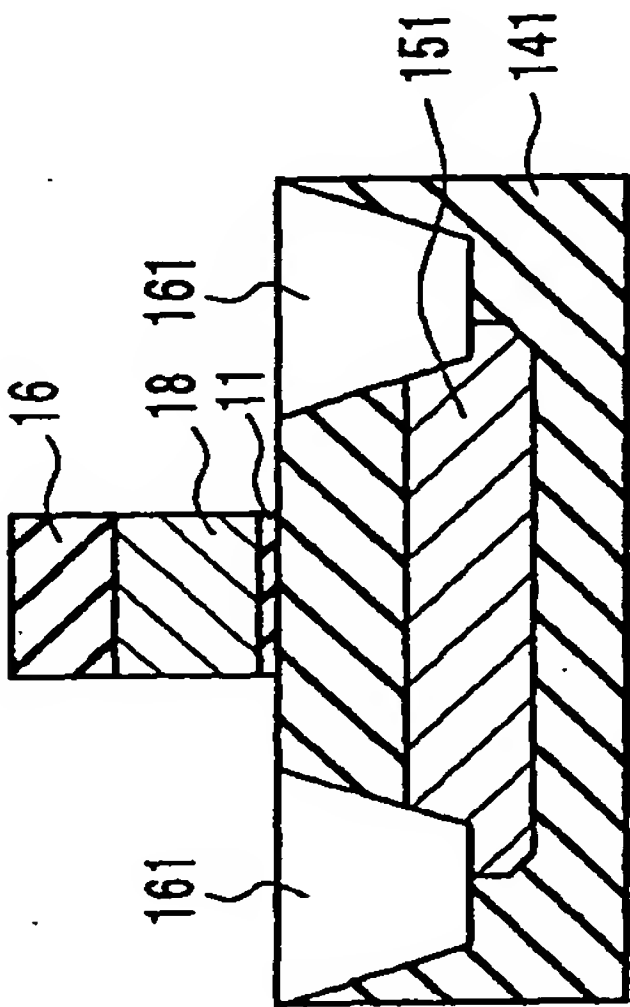


FIG. 9C  
PRIOR ART

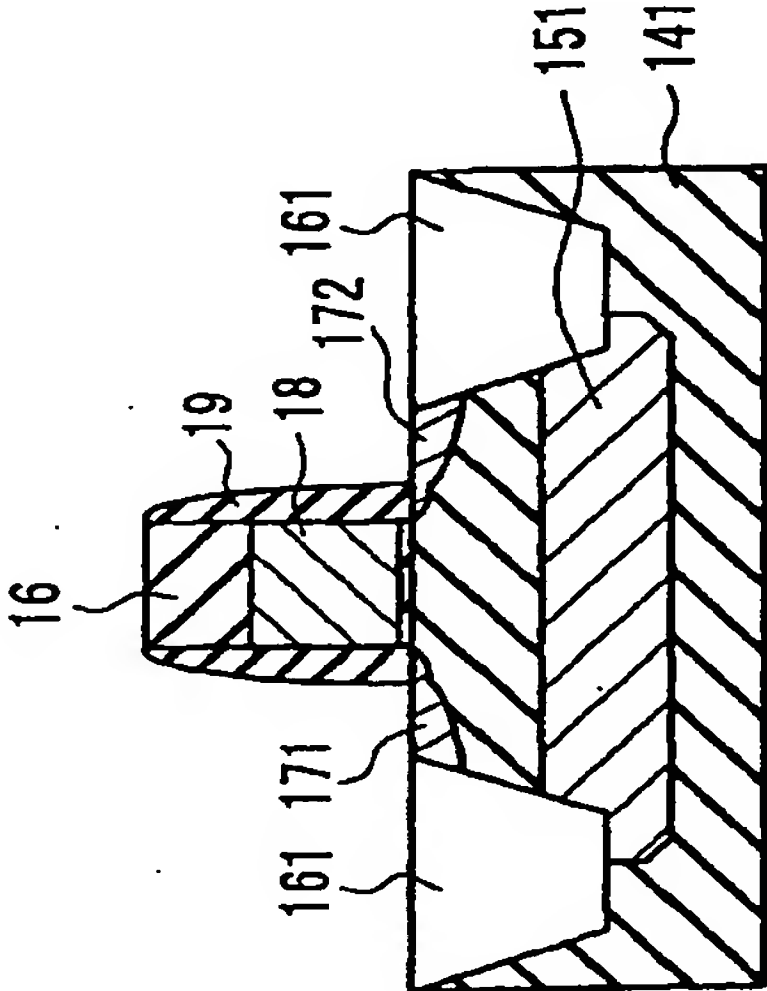


FIG. 9D  
PRIOR ART

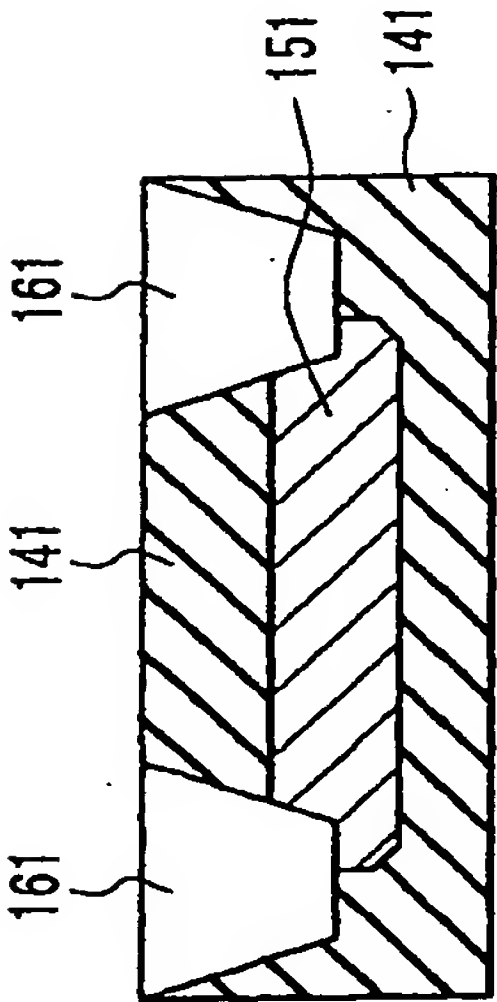


FIG. 9A  
PRIOR ART

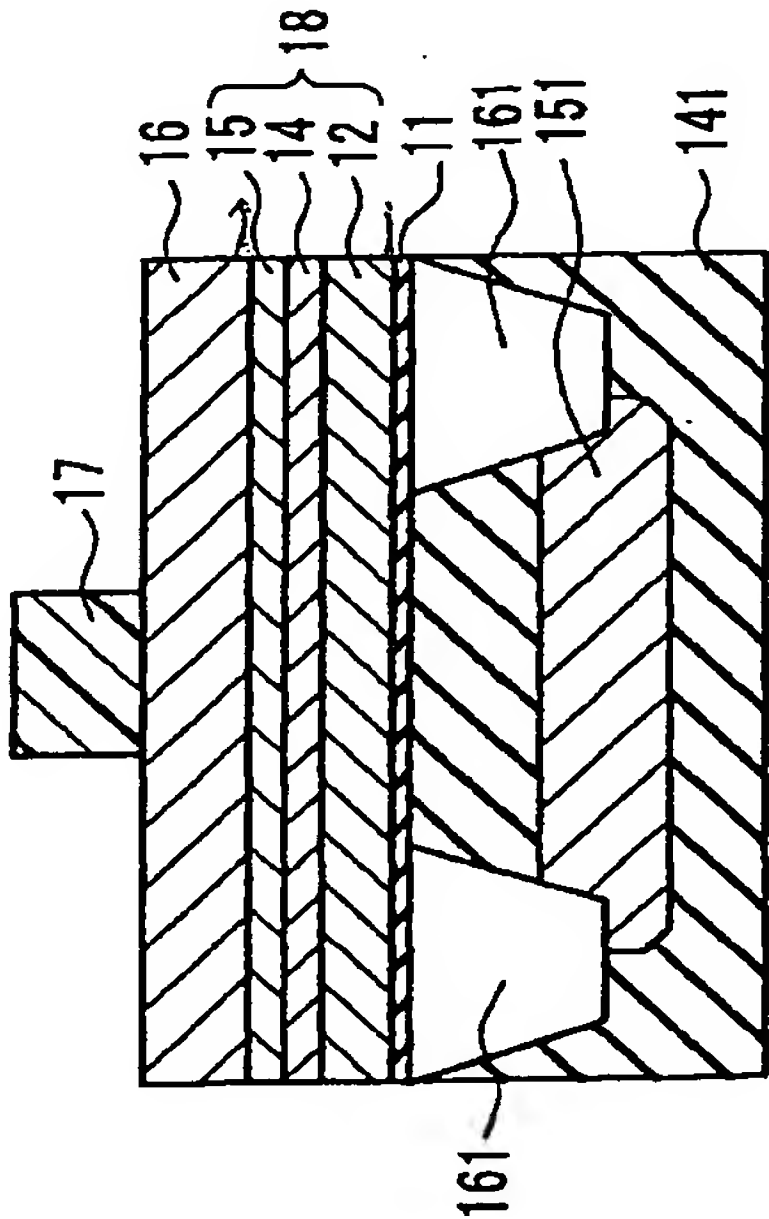


FIG. 9B  
PRIOR ART

EP 1 347 503 A2

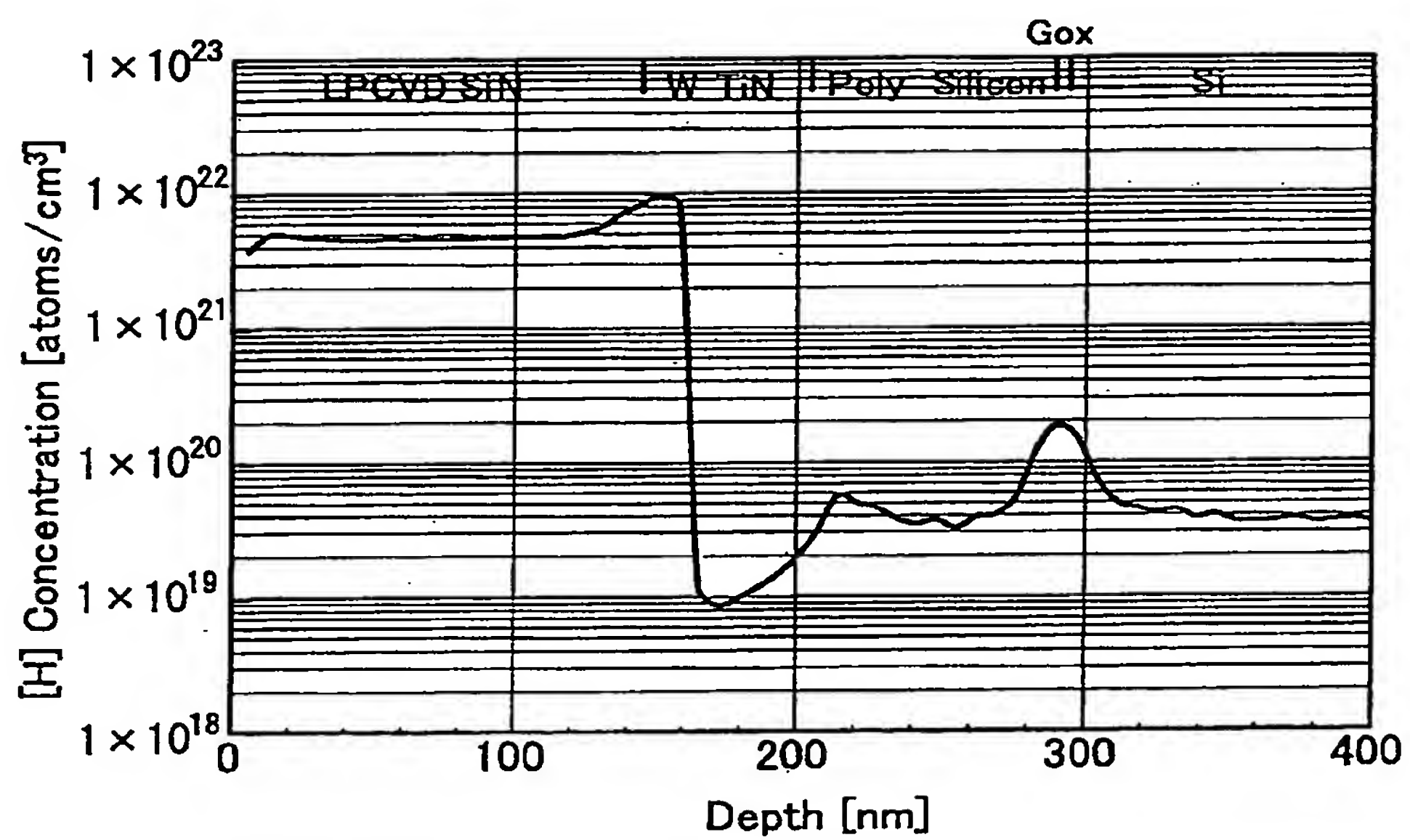


FIG. 10  
PRIOR ART

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